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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,398	11/30/2001	Colin D. Yates	01-234	5786

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EXAMINER	
LAUCHMAN, LAYLA G	

ART UNIT	PAPER NUMBER
2877	

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,398	YATES ET AL.	
	Examin r	Art Unit	
	L. G. Lauchman	2877	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *07 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-16,18,20,21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziger (US 6,498,640), and further in view of Stirton et al (US 6,614,540).

As to Claim 1, Ziger discloses a method of measuring alignment in a semiconductor fabrication process that uses underlying and latent images on a substrate, comprising:

forming a test pattern in selected fields of a first layer on a semiconductor substrate (Fig. 2A, see col. 5, lines 46-48);

forming a layer of photoresist over said first layer (see col. 5, lines 50-51);

forming latent images in portions of said photoresist in said photoresist layer lying in said selected fields overlying said test pattern of said first layer (see Fig. 2B, col. 5, lines 53-63);

measuring the alignment of said test pattern in said selected fields of said first layer with said overlaying latent images in said photoresist (see col. 3, lines 10-15 and col 5. lines 64-66).

Ziger does not specifically disclose that measuring alignment of said test pattern and said overlying latent images is carried out by using scatterometry.

Scatterometry is well known (as admitted in the specifications) and refers to a procedure in which light of a specific wavelength is scattered of gratings in various directions known as orders. The light diffracted off the gratings is interpreted to determine the line profiles within the gratings.

The patent '540 to Stirton et al teach a method of measuring misalignment errors between semiconductor layers based upon scatterometric measurements. Therefore, it would have been obvious to measure alignment of the test pattern and the latent images in the invention of Ziger using scatterometry, since the test pattern and the latent images in Ziger's patent represent grating images (col. 6, lines 20-44), which make scatterometric measurement feasible according to the definition of scatterometry.

As to Claims 2 and 3, the patents '640 and '540 teach all as applied to Claim 1 above, in addition said test pattern of the first layer comprises a test pattern of lines, and the test pattern of lines comprises a test pattern of parallel space apart lines (see Fig. 2A).

As to Claim 4, the patents '640 and '540 teach all as applied to Claim 2 above, in addition the grating pattern of the patent '540 teaches the grating pattern being formed of metal lines (see col. 5. lines 50-67).

As to Claim 5, the patents '640 and '540 teach all as applied to Claim 3 above, in addition the latent images overlying the test pattern of lines comprises a pattern of parallel spaced apart lines (se Fig. 2B).

As to Claim 6, the patents '640 and '540 teach all as applied to Claim 5 above, in addition said latent images of parallel spaced apart lines, formed in said portions of said photoresist layer lying in the selected fields overlying said test pattern of parallel spaced apart lines of first layer, are formed generally parallel to said test pattern, whereby the test pattern and said latent images form a diffraction grating, the accuracy of which can

be measured by said scatterometry to determine the alignment of the layers (col. 6, lines 20-44).

As to Claim 7, the patents '640 and '540 teach all as applied to Claim 6 above, in addition said latent images are interspaced between said test pattern (see Fig. 2B).

Claims 8-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ziger (US 6,498,640), and further in view of Stirton et al (US 6,614,540).

As to Claim 8, Ziger discloses a method of measuring alignment in a semiconductor fabrication process that uses underlying and latent images on a substrate, comprising:

forming a test pattern of parallel spaced apart lines in selected fields of a first layer on a semiconductor substrate (Fig. 2A, see col. 5, lines 46-48) ;

forming a layer of photoresist over said first layer (see col. 5, lines 50-51);

forming latent images of parallel spaced apart lines in portions of said photoresist in said photoresist layer lying in said selected fields overlying said test pattern of said first layer , said parallel lines of the test pattern of said first layer generally parallel with said parallel lines of latent images (see Fig. 2B, col. 5, lines 53-63, col. 6, lines 20-44);

measuring the alignment of said test pattern in said selected fields of said first layer with said overlaying latent images in said photoresist (see col. 3, lines 10-15 and col 5. lines 64-66).

Ziger does not specifically disclose that measuring alignment of said test pattern and said overlying latent images is carried out by using scatterometry.

Scatterometry is well known (as admitted in the specifications) and refers to a procedure in which light of a specific wavelength is scattered of gratings in various directions known as orders. The light diffracted off the gratings is interpreted to determine the line profiles within the gratings.

The patent '540 to Stirton et al teach a method of measuring misalignment errors between semiconductor layers based upon scatterometric measurements. Therefore, it would have been obvious to measure alignment of the test pattern and the latent images in the invention of Ziger using scatterometry, since the test pattern and the latent images in Ziger's patent represent grating images (col. 6, lines 20-44), which make scatterometric measurement feasible according to the definition of scatterometry.

As to Claim 9, the patents '640 and '540 teach all as applied to Claim 8 above, in addition the grating pattern of the patent '540 teaches the grating pattern being formed of metal lines (see col. 5. lines 50-67).

As to Claim 10, the patents '640 and '540 teach all as applied to Claim 8 above, in addition said latent images of parallel spaced apart lines, formed in said portions of said photoresist layer lying in the selected fields overlying said test pattern of parallel spaced apart lines of first layer, are formed generally parallel to said test pattern, whereby the test pattern and said latent images form a diffraction grating, the accuracy of which can be measured by said scatterometry to determine the alignment of the layers (col. 6, lines 20-44).

As to Claim 11, the patents '640 and '540 teach all as applied to Claim 10 above, in addition said latent images are interspaced between said test pattern (see Fig. 2B).

As to Claim 12, the patents '640 and '540 teach all as applied to Claim 8 above, in addition the step of forming latent images comprises directing a first source of radiation 4 onto the photoresist layer through a reticle 8 patterned to provide a radiation image of said parallel lines. (see col. 4, lines 53-68)

As to Claims 13, 15, and 16, the patents '640 and '540 teach all as applied to Claim 12, except that the step of measuring the alignment of the test pattern and the latent images comprises a second light source, which comprises visible light source or a laser beam. The patent '540 teaches the white (visible) light source (col. 9, lines 1-5) for carrying out the scatterometric measurements. It would have been obvious to one skilled in the art to use a second light source, i.e. a laser beam of visible light, in the invention of Ziger for conducting scatterometric measurements, since conventional scatterometry apparatuses require radiation sources with a wavelength at which the photoresist layer is not sensitive to avoid exposing the entire photoresist layer to radiation used to for the latent image.

As to Claim 14, the patents '640 and '540 teach all as applied to Claim 12, however, Ziger is silent on the type of light used in the invention. It is known that photoresist is generally a composition that is sensitive to active rays of light (for example, see US patent 6, 259,521, col.1, second paragraph) such as ultraviolet rays. Therefore, it would have been obvious to one skilled in the art to have ultraviolet light as

the first light in the invention of Ziger, since that type of active light would form the latent images in the photoresist layer.

As to Claim 18, Ziger discloses a method of measuring alignment in a semiconductor fabrication process that uses underlying and latent images on a substrate, comprising:

forming a test pattern of parallel spaced apart lines in selected fields of a first layer on a semiconductor substrate (Fig. 2A, see col. 5, lines 46-48) ;

forming a layer of photoresist over said first layer (see col. 5, lines 50-51);

forming latent images of parallel spaced apart lines in portions of said photoresist in said photoresist layer lying in said selected fields overlying said test pattern of said first layer , said parallel lines of the test pattern generally parallel with said parallel lines of latent images (see Fig. 2B, col. 5, lines 53-63, col. 6, lines 20-44);

measuring the alignment of said test pattern in said selected fields of said first layer with said overlaying latent images in said photoresist (see col. 3, lines 10-15 and col 5. lines 64-66).

Ziger does not specifically disclose that measuring alignment of said test pattern and said overlying latent images is carried out by using scatterometry.

Scatterometry is well known (as admitted in the specifications) and refers to a procedure in which light of a specific wavelength is scattered of gratings in various directions known as orders. The light diffracted off the gratings is interpreted to determine the line profiles within the gratings.

The patent '540 to Stirton et al teach a method of measuring misalignment errors between semiconductor layers based upon scatterometric measurements. Therefore, it would have been obvious to measure alignment of the test pattern and the latent images in the invention of Ziger using scatterometry, since the test pattern and the latent images in Ziger's patent represent grating images (col. 6, lines 20-44), which make scatterometric measurement feasible according to the definition of scatterometry.

Ziger does not specifically disclose the step of forming a further layer of integrated circuit over said first layer on said integrated circuit structure in fields not used for said alignment.

It would have been obvious to one skilled in the art to form a further layer of integrated circuit over the first layer of the integrated circuit structure of the Ziger's invention in the field not used for said alignment or, in other words, to form another set of test fields on a wafer, in order to verify that the detected and corrected misalignment in the first test fields is satisfactory. The motivation for doing so is to avoid the need for expenditure of an entire test wafer to verify the alignment and also permit each individual wafer to be tested for alignment.

As to Claim 20 and 21, Ziger discloses a method of measuring alignment in a semiconductor fabrication process that uses underlying and latent images on a substrate, comprising:

forming a test pattern of parallel spaced apart lines in selected fields of a first layer on a semiconductor substrate (Fig. 2A, see col. 5, lines 46-48) ;

forming a layer of photoresist over said first layer (see col. 5, lines 50-51);

forming latent images of parallel spaced apart lines in portions of said photoresist in said photoresist layer lying in said selected fields overlying said test pattern of said first layer , said parallel lines of the test pattern generally parallel with said parallel lines of latent images (see Fig. 2B, col. 5, lines 53-63, col. 6, lines 20-44);

measuring the alignment of said test pattern in said selected fields of said first layer with said overlaying latent images in said photoresist (see col. 3, lines 10-15 and col 5. lines 64-66).

Ziger does not specifically disclose that measuring alignment of said test pattern and said overlying latent images is carried out by using scatterometry.

Scatterometry is well known (as admitted in the specifications) and refers to a procedure in which light of a specific wavelength is scattered of gratings in various directions known as orders. The light diffracted off the gratings is interpreted to determine the line profiles within the gratings.

The patent '540 to Stirton et al teach a method of measuring misalignment errors between semiconductor layers based upon scatterometric measurements. Therefore, it would have been obvious to measure alignment of the test pattern and the latent images in the invention of Ziger using scatterometry, since the test pattern and the latent images in Ziger's patent represent grating images (col. 6, lines 20-44), which make scatterometric measurement feasible according to the definition of scatterometry.

It would have been obvious to one skilled in the art to use the remaining fields of the integrated circuit structure of the Ziger's invention to be conventionally processed to form semiconductor structures, in order to avoid the need for expenditure of an entire

test wafer to verify the alignment and also permit each individual wafer to be tested for alignment.

Response to Arguments

Applicant's arguments filed 1/7/2004 have been fully considered but they are not persuasive.

In response to applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The applicants assert that nothing in the cited references suggests the novel combination of steps. However, the patent to Stirton clearly suggests the use of scatterometry to measure alignment between a first grating structure that could be a test pattern and a second grating structure, which is defined as a latent photoresist pattern. The system also subsequently corrects the alignment error (see col. 6, lines 9-31)

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to TC 2877 via the PTO Fax Center located in CP4-4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The CP4 Fax Center number is (703) 872-9306.

If the Applicant wishes to send a Fax dealing with either a Proposed Amendment or for discussion for a phone interview then the fax should:

a) Contain either the statement "DRAFT" or "PROPOSED AMENDMENT" on the Fax Cover Sheet; and

b) Should be unsigned by the attorney or agent.

This will ensure that it will not be entered into the case and will be forwarded to the examiner as quickly as possible.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to L. G. Lauchman whose telephone number is (571) 272-2418.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC receptionist whose telephone number is (571) 272-1562.

L. G. Lauchman
Patent Examiner
Art Unit 2877
4/22/04/lgl

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